

A LATERAL CAPACITIVE CMOS ACCELEROMETER WITH STRUCTURAL CURL COMPENSATION

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ABSTRACT

We present successful experimental results from the first lateral capacitive accelerometer to be designed and manufactured in a conventional CMOS process. Compatibility with conventional CMOS provides advantages of low cost, high yield and fast prototyping that should be transferable to any CMOS foundry. A fully differential capacitive-bridge interface which can not be realized in polysilicon technology is designed and implemented. Out-of-plane curling associated with the composite structural layers is compensated to first order through a curl matching technique. The prototype accelerometer has a measured sensitivity of 1.2 mV/g and a 0.5 mg/rtHz noise floor at the output of the sensing element.

INTRODUCTION

Accelerometers fabricated with high-aspect-ratio CMOS micromachining have advantages of being 100% compatible with conventional integrated-circuit technology and utilizing silicon area efficiently, leading to very low cost [1][2]. On-chip capacitive displacement sensors exhibit very low parasitic capacitance and the ability to place multiple isolated conductors in microstructures allows design of fully differential sensing and actuation.

Comparatively, commercial monolithic integrated microaccelerometers are made from custom processes that combine polysilicon surface micromachining and electronic circuits processes [3]. Microstructures are separated from electronics by approximately 100 μm due to process limitations, which wastes a significant amount of silicon area. Parasitic capacitance between the structural layer to the substrate can be in the order of several pF for a typical inertial sensor design. Therefore driven shielding is often used to reduce effective parasitic capacitance and increase sensitivity. Interconnect for microstructures and electronics is implemented by a polysilicon layer or

by diffusion with large resistivity which results in large wiring thermal noise. Extra micromachining process steps usually involve performance and yield compromises and are incompatible with standard IC technology.

Previous works have utilized two kinds of sense interfaces for the sensing element in the accelerometers. One kind is the single-ended half-bridge interface as shown in Figure 1(a)[4]. The second kind, fully differential interfaces, are always preferred to their single-ended counterparts because of better power supply rejection and first-order cancellation of substrate coupling. Illustrated in Figure 1(b) is a differential capacitive sense interface configured as a capacitive half-bridge implemented with a polysilicon surface micromachining process [5]. A significant common-mode modulating signal will appear at the output nodes of the differential interface, since there is only one modulation node. Special input common-mode feedback (ICMFB) circuitry improves input common-mode rejection ratio (ICMRR) and dynamic range of the interface electronics, at the expense of noise and bandwidth. Mismatch in parasitic capacitors and feedback capacitors results in output offset which can be a great source of drift over environmental variations, such as temperature and aging.

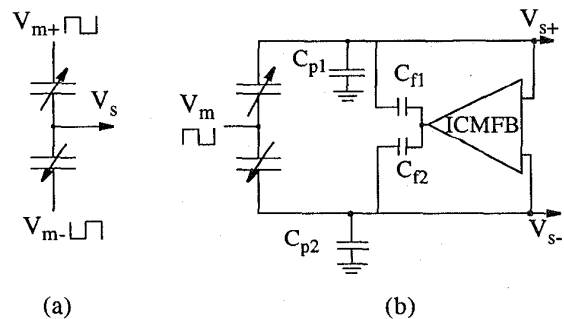


Figure 1. Capacitive interfaces with polysilicon process. (a) single-ended and (b) differential configuration.

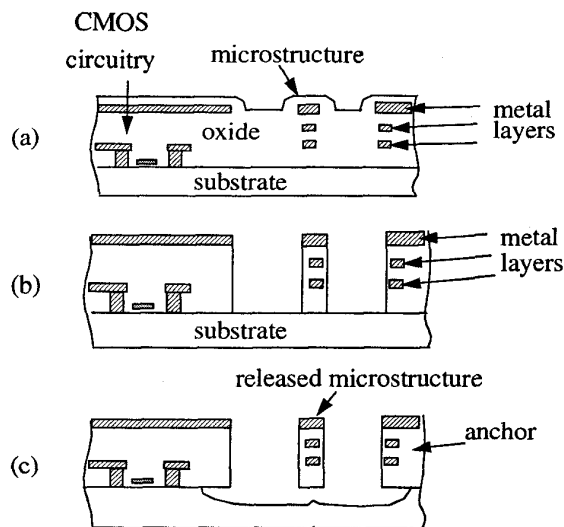


Figure 2. Cross sections of CMOS-MEMS process flow. (a) After CMOS process. (b) After anisotropic dielectric etch. (c) After bulk silicon etch for release.

Exploiting the advantage of multiple isolated conductors in the composite structural layers, a fully differential capacitive full-bridge interface is easily implemented with CMOS micromachining process eliminating the problem of ICMRR.

One of the challenges in design with the CMOS micromachining process is the larger residual-stress gradient associated with the composite metal-dielectric structural layers. Microstructures with dimension larger than $100\ \mu\text{m}$ can curl out-of-plane noticeably. A structural curl compensation technique is proposed in this paper to address this problem.

CMOS MICROMACHINING PROCESS

The accelerometer described in this paper is fabricated with a high-aspect-ratio CMOS micromachining technology [1][2]. The process flow, shown in Figure 2, incorporates microstructures with the Hewlett-Packard $0.5\ \mu\text{m}$ three-metal n-well CMOS process. After the foundry CMOS processing, two steps of maskless dry etches, with the top metal layer as etch resistant mask, are performed to create microstructures. An anisotropic reactive ion etch (RIE) with CHF_3/O_2 is first performed to etch away exposed oxides, and form microstructural side-walls. This step is followed by a more isotropic RIE with

SF_6/O_2 to etch bulk silicon and release the microstructures from substrate. Dry etches eliminate sticking problems associated with competing wet-etch release processes.

CMOS micromachining technology has many advantages over polysilicon surface-micromachining processes. Compatibility with conventional CMOS technology enables fast, repeatable, reliable, and economical fabrication of MEMS devices integrated with conventional CMOS. Microstructures can be integrated as close as $12\ \mu\text{m}$ from on-chip electronics limited by the silicon undercuts. Since the mask metal layer is defined by lithography in the CMOS process, the minimum microstructure feature size scales with CMOS technology. Structural layers are released with a gap of more than $20\ \mu\text{m}$ above the substrate, providing a much smaller parasitic capacitance to the substrate. Aluminum interconnect practically eliminates thermal noise caused by wiring resistance. Multiple conductors can be built into structural layers, which allow novel and flexible designs, such as fully differential capacitive sensors as described in this paper, self-actuating springs [1] and gimballed gyroscopes [6]. Such designs can not be implemented in homogeneous conducting structural layers such as those in polysilicon technology.

FULLY DIFFERENTIAL ACCELEROMETER DESIGN

Schematic views of the accelerometer and the fully differential, full-bridge, capacitive sense interface are shown in Figure 3. The proof mass is suspended by four-meander springs connected at each corner. Each meander beam in layout is $2.1\ \mu\text{m}$ wide and $147.3\ \mu\text{m}$ long. Motion of the proof mass is in the y direction. The suspension springs and stator fingers are anchored on the rigid frame which is anchored to the substrate on two ends. Each capacitor shown in Figure 3(a) comprises nine interdigitated comb fingers with $53.4\ \mu\text{m}$ -long $1.5\ \mu\text{m}$ -wide gaps. The micromechanical topology is similar to that of Analog Devices' ADXL05 device [3], however there are important differences in the wiring and stator mechanics. The two modulation signals, V_{m+} and V_{m-} , are routed to the proof mass through the suspension springs. The stator sensing fingers and the suspension springs are anchored to a rigid frame which is suspended $20\ \mu\text{m}$ above the substrate. The high-impedance sense nodes, V_{s+} and V_{s-} , are routed through the suspended

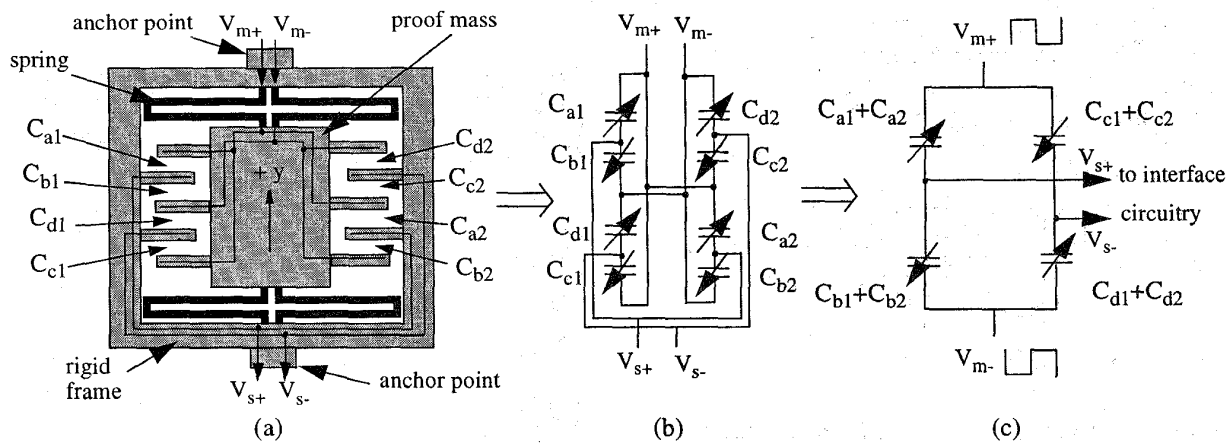


Figure 3. Capacitive displacement sensing interface of the accelerometer, illustrating the common-centroid and fully differential features. (a) Notional top view of the layout with eight sense capacitors. (b) Equivalent electrical schematic. (c) Reduced electrical schematic.

rigid frame to the following electronics. This arrangement minimizes parasitic capacitance to the substrate.

This topology can approximately double the sensitivity of the half-bridge topology with the same value of sensing capacitance. Since the interface is truly fully differential, high CMRR can be achieved at the outputs. There is no need for extra circuitry for ICMFB at the inputs of sensing electronics.

A common-centroid topology is utilized to minimize cross-axis sensitivity. Sensing fingers are split into four groups of differential capacitor pairs. The upper-left group and lower-right group are connected to form one half of capacitor-bridge, and the upper-right group and lower-left group to form the other half. Displacement along the y-axis will cause capacitors to change as shown in Figure 3, resulting in a differential output. Cross-axis translations and rotations either are rejected by the common-centroid layout to first order or cause only a common-mode signal which is rejected by the following differential electronic circuitry. As shown in Figure 4, fully differential front-end interface circuitry consisting of unity-gain buffers [4] and pre-amplifiers is integrated with the prototype accelerometer. Diodes are used at the inputs of the buffers to provide DC bias. No driven shielding is used due to small parasitic capacitance.

STRUCTURAL CURL COMPENSATION

Composite metal-dielectric structural layers

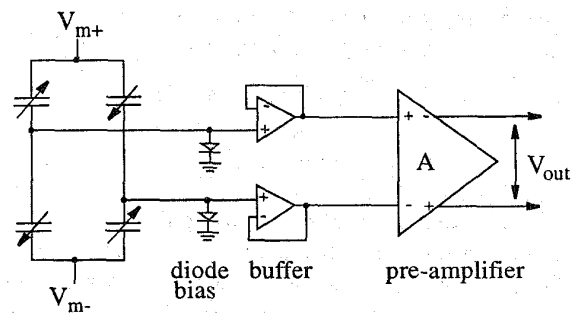


Figure 4. Schematic of on-chip sensor and circuitry.

made from the CMOS interconnect experience larger vertical stress gradient than their homogenous polysilicon counterpart and tend to curl out-of-plane. The typical radius of curvature of the structural layer can be relatively small, between 1 mm to 5 mm, compared with a radius of curvature at the order of hundreds of millimeters in an optimized polysilicon surface-micromachining technology [7].

Without proper design, proof-mass fingers and stator fingers will curl in opposing directions as shown in Figure 5(a) and the sidewall sensing capacitance will be significantly reduced. Moreover, the sidewall capacitance will change dramatically with temperature and from run to run [8]. The design technique shown in Figure 5(b) takes advantage of good local matching of curl to solve

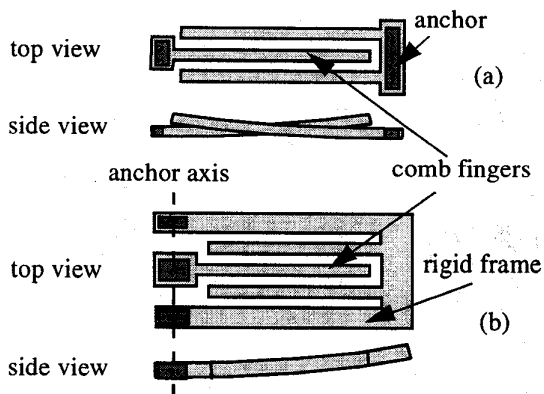


Figure 5. Curl matching technique for comb-fingers. (a) Without curl matching, (b) With curl matching.

the problem of indeterminate sidewall capacitance. The stator and proof-mass fingers are anchored along a common axis, with the stator connected to a cantilevered frame that is rigid compared with the proof-mass suspension. As a result, the interdigitated fingers will curl in line and provide maximum sidewall capacitance.

RESULTS

Devices were fabricated using the Hewlett-Packard 0.5 μm 3-metal CMOS process available through MOSIS. A top view of the accelerometer is shown in Figure 6. The sensing element measures 400 μm by 450 μm . The proof mass is perforated for release. Electrostatic self-test actuators are located on the four corners. On-chip electronic circuitry is covered by top metal-3 layer and can not be seen from the SEM picture. The chip with the buffer and preamplifier electronics is 500 μm x 850 μm , however the layout has not been optimized for area minimization. Figure 7 shows a side view of the device. The interdigitated sense fingers curl up in line with the rigid suspension frame.

Design parameters and measured performance of the accelerometer are summarized in Table 1. A small parasitic capacitance of 60 fF to ground is present at each of the high-impedance sensor nodes. The measured sense capacitance is smaller than predicted by 32%. Mismatch between the plate-mass composite material and the rigid-frame material produces vertical misalignment between the rotor and stator fingers. An enlargement of the corner of the accelerometer in Figure 8 shows the vertical mis-

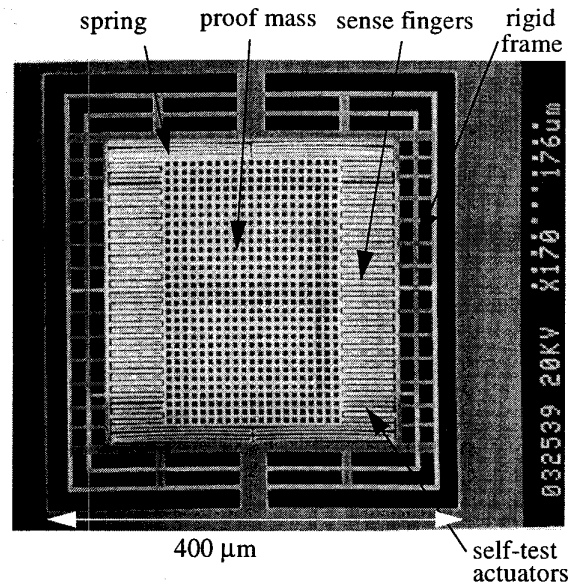


Figure 6. SEM of the top view of the accelerometer.

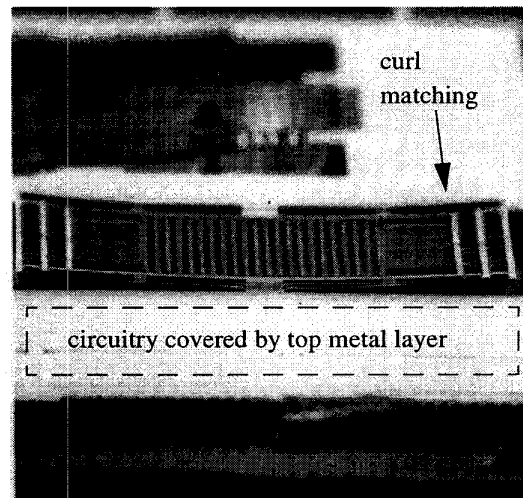


Figure 7. SEM showing the side profile of the accelerometer. Curling out of plane is evident. The stator and rotor fingers match in curl to first order.

alignment. The rotor fingers are shifted down approximately 2.5 μm with respect to the stator fingers, which results in the reduced sidewall sensing capacitance. Lateral etch during the microstructural RIE increases the gap by between 0.3 μm to 0.6 μm and further lowers the value of sense capacitance.

Table 1: Parameters of the accelerometer

Parameter	Design	Measured
Spring constant	0.5 N/m	-
Proof mass	0.45 μg	-
Resonant frequency	5.3 kHz	4.8 kHz
Sensing capacitance	80 fF	26 fF *
Parasitic capacitance	120 fF	120 fF *
Sensitivity	1.7 mV/g/V	1.2 mV/g/V
Noise floor	0.37 mg/rtHz	0.5 mg/rtHz
Cross-sensitivity	0	< -30dB
Q factor in air	-	8

* measured ratio of $C_{\text{sense}}/C_{\text{parasitic}}$

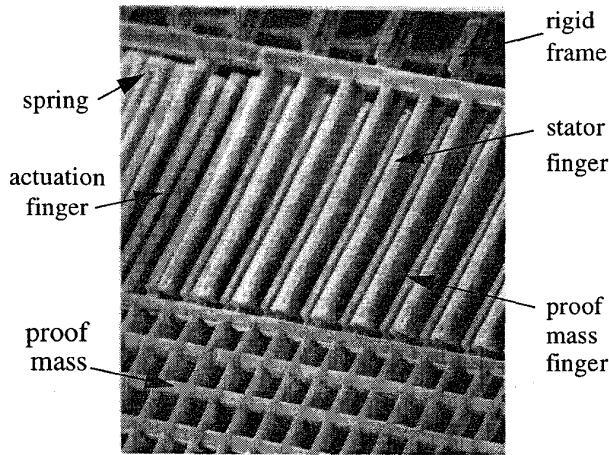


Figure 8. A corner of the device. Fingers on the proof mass are approximately $2.5 \mu\text{m}$ lower than stator fingers resulting in smaller sense capacitance.

Spectral response of the accelerometer, shown in Figure 9, was obtained by applying a 1g sinusoidal acceleration signal with a calibrated shaker table. The noise floor is 0.5 mg/rtHz. Frequency response of the sensor, as shown in Figure 10, was obtained by applying a sinusoidal voltage to the self-test actuator. The resonance frequency of 4.8 kHz matches the design value. The quality factor of 8 is due to squeeze damping of the fingers.

A mechanical offset of around $0.4 \mu\text{m}$ is present in the device due to lateral curling of the suspension beams,

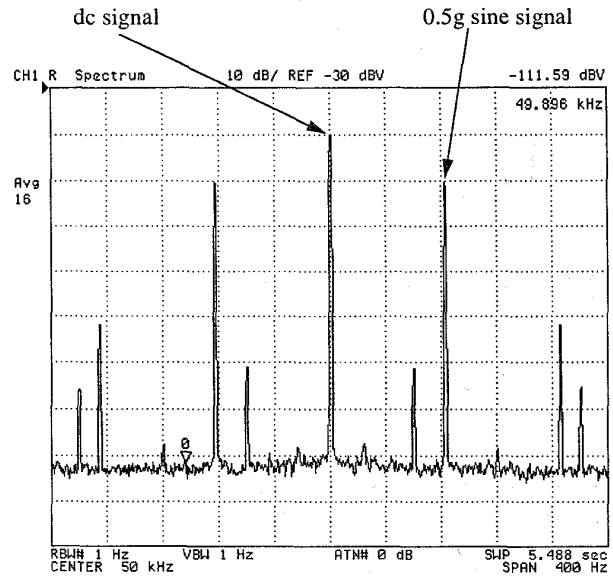


Figure 9. Spectrum of the modulated output signal at the pre-amp output due to an 80 Hz 1 g sinusoidal input. The noise floor is 0.5 mg/rtHz. The other peaks are higher order harmonics and 60 Hz power line noise.

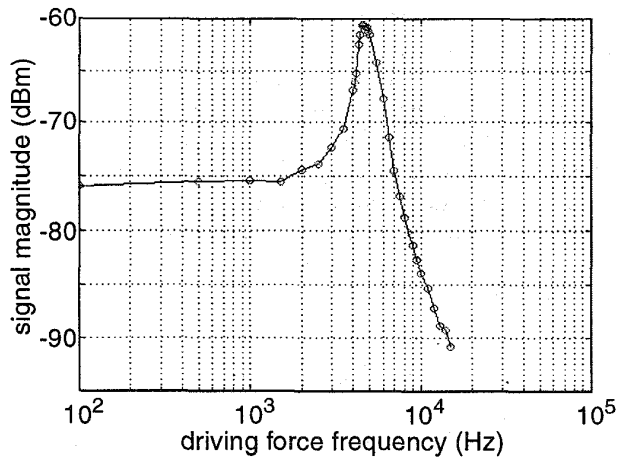


Figure 10. Frequency response of the accelerometer driven with the self-test actuators. Resonance occurs at 4.8 kHz.

which are thinned to a $1.5 \mu\text{m}$ width by the dielectric RIE. The offset was partially cancelled by a 24 V dc voltage applied to the self-test actuators. The large mechanical offset present in the sensor is attributed to the lateral curling of the suspension springs. The lateral curling is

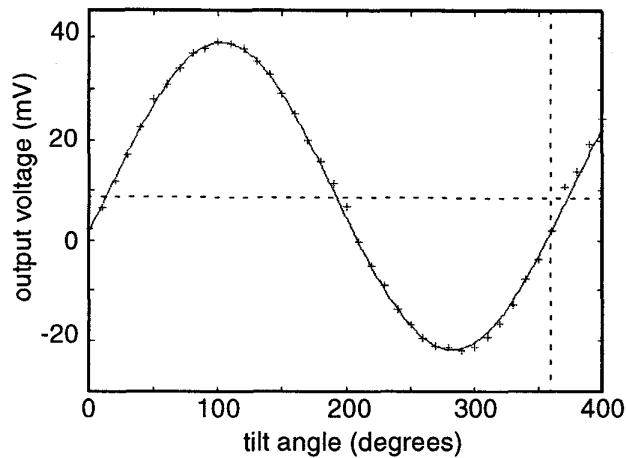


Figure 11. Tilt measurements, measured at one output of the pre-amplifiers. A dc bias of 8 mV is evident. The plot is corrected for bias drift that is linear in time.

an effect unique to high-aspect-ratio CMOS processing caused by manufacturing misalignment of the inner film layers coupled with the very small beam stiffness. This problem can be relieved by improved lithography alignment, and with optimal layout of the metal layers inside the beams. Reducing the number of spring meanders and widening the suspension beams will help to reduce the offset, but the sensitivity is also reduced.

The static response to gravity, shown in Figure 11, was measured using a precision rotary stage. A bias (offset) drift of around 0.2mV/min/V is present during the experiment. The tilt data in Figure 11 is corrected by assuming drift that changes linearly with time. The drift is believed to be due to moving contact between the suspension beams, and should be reduced in second-generation designs.

CONCLUSIONS

We have demonstrated that relatively high-performance capacitive accelerometers can be made directly in a conventional CMOS process. Since there are no special process steps inserted into the CMOS flow, very low cost accelerometers may be fabricated. Large residual-stress gradient is present in the composite structural layers, however, curl matching techniques can compensate out-of-plane curl to first order. Manufacturing misalignment of metal layers causes lateral stress gradient in the microstructures, which results in large DC offset in the accelerometer. This calls for further research on design

techniques to ensure negligible effects from residual stress and curling.

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